

M5M5V208FP,VP,RV,KV,KR -70L, -85L, -10L, -12L, -70LL, -85LL, -10LL, -12LL

PRELIMINARY

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Some parametric limits are subject to change.

2097152-BIT (262144-WORD BY 8-BIT) CMOS STATIC RAM

DESCRIPTION

The M5M5V208 is 2,097,152-bit CMOS static RAM organized as 262,144-words by 8-bit which is fabricated using high-performance quadruple-polysilicon and double metal CMOS technology. The use of thin film transistor(TFT) load cells and CMOS periphery results in a high density and low power static RAM. The M5M5V208 is designed for memory applications where high reliability, large storage, simple interfacing and battery back-up are important design objectives.

The M5M5V208VP,RV,KV,KR are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD). Two types of devices are available.

VP,KV(normal lead bend type package),RV,KR(reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURE

Type	Access time (max)	Power supply current	
		Active (max)	Stand-by (max)
M5M5V208FP,VP,RV,KV,KR-70L	70ns	27mA (V _{cc} =3.6V)	60μA (V _{cc} =3.6V)
M5M5V208FP,VP,RV,KV,KR-85L	85ns		
M5M5V208FP,VP,RV,KV,KR-10L	100ns		
M5M5V208FP,VP,RV,KV,KR-12L	120ns		
M5M5V208FP,VP,RV,KV,KR-70LL	70ns	10μA (V _{cc} =3.6V)	
M5M5V208FP,VP,RV,KV,KR-85LL	85ns		
M5M5V208FP,VP,RV,KV,KR-10LL	100ns		
M5M5V208FP,VP,RV,KV,KR-12LL	120ns		

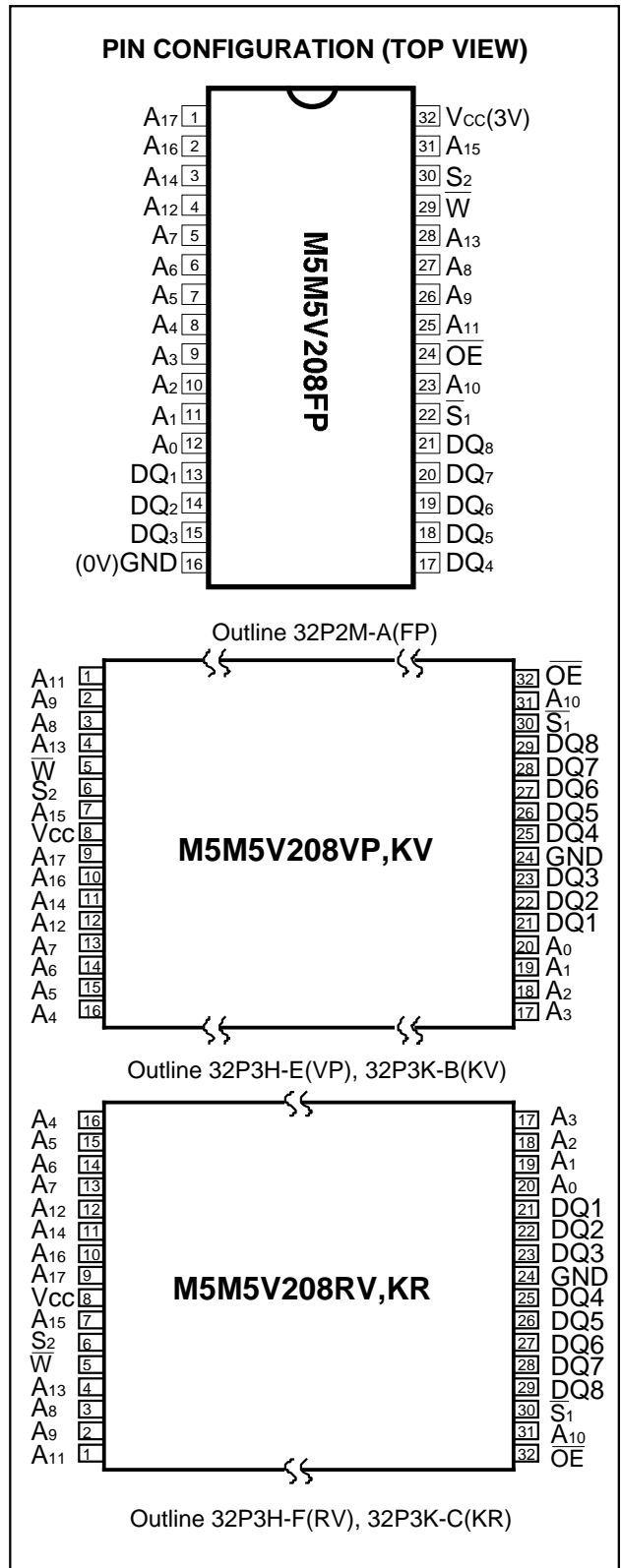
- Single 2.7 ~ 3.6V power supply
- Operating temperature of 0 to +70°C
- No clocks, No refresh
- All inputs and outputs are TTL compatible.
- Easy memory expansion and power down by S1 & S2
- Data retention supply voltage=2.0V
- Three-state outputs: OR-tie capability
- OE prevents data contention in the I/O bus
- Common Data I/O
- Battery backup capability
- Small stand-by current 0.3μA(typ.)

PACKAGE

- M5M5V208FP : 32 pin 525 mil SOP
- M5M5V208VP,RV : 32pin 8 X 20 mm² TSOP
- M5M5V208KV,KR : 32pin 8 X 13.4 mm² TSOP

APPLICATION

- Small capacity memory units
- Battery operating system
- Handheld communication tools



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FUNCTION

The operation mode of the M5M5V208 is determined by a combination of the device control inputs $\overline{S_1}$, S_2 , \overline{W} and \overline{OE} . Each mode is summarized in the function table.

A write cycle is executed whenever the low level \overline{W} overlaps with the low level $\overline{S_1}$ and the high level S_2 . The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of \overline{W} , $\overline{S_1}$ or S_2 , whichever occurs first, requiring the set-up and hold time relative to these edge to be maintained. The output enable \overline{OE} directly controls the output stage. Setting the \overline{OE} at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

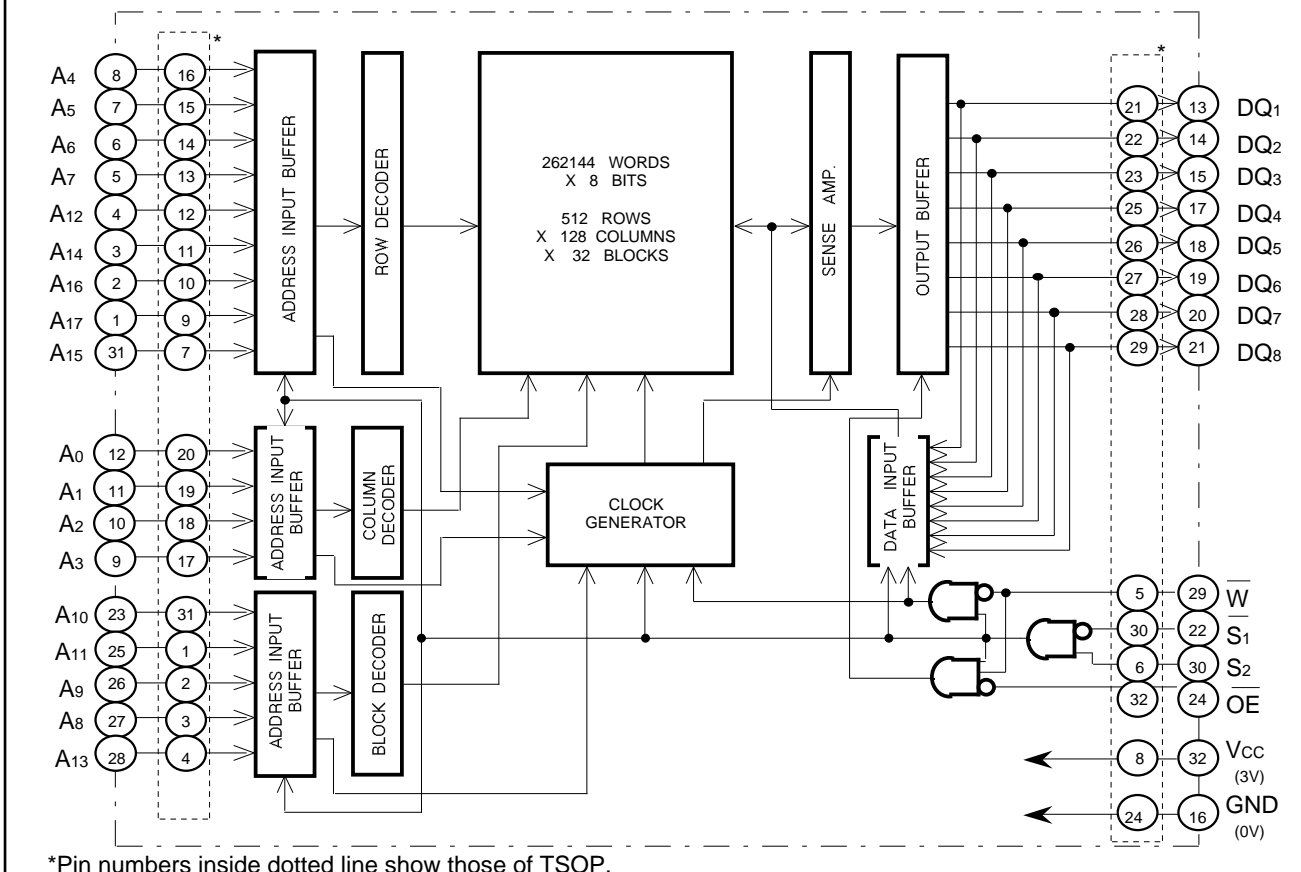
A read cycle is executed by setting \overline{W} at a high level and \overline{OE} at a low level while $\overline{S_1}$ and S_2 are in an active state ($S_1 = L, S_2 = H$).

When setting $\overline{S_1}$ at a high level or S_2 at a low level, the chips are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high-impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S_1}$ or S_2 . The power supply current is reduced as low as the stand-by current which is specified as I_{cc3} or I_{cc4} , and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S_1}$	S_2	\overline{W}	\overline{OE}	Mode	DQ	I_{cc}
X	L	X	X	Non selection	High-impedance	Standby
H	X	X	X	Non selection	High-impedance	Standby
L	H	L	X	Write	D _{IN}	Active
L	H	H	L	Read	D _{OUT}	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V _{cc}	Supply voltage	With respect to GND	- 0.5*~4.6	V
V _I	Input voltage		- 0.5* ~ V _{cc} + 0.5 (Max 4.6)	V
V _O	Output voltage		0 ~ V _{cc}	V
P _d	Power dissipation	T _a =25°C	700	mW
T _{opr}	Operating temperature		0 ~ 70	°C
T _{str}	Storage temperature		- 65 ~150	°C

* -3.0V in case of AC (Pulse width 30ns)

DC ELECTRICAL CHARACTERISTICS

(T_a=0~70°C, V_{cc}= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{IH}	High-level input voltage		2.0		V _{cc} +0.3V	V
V _{IL}	Low-level input voltage		-0.3*		0.6	V
V _{OH1}	High-level output voltage 1	I _{OH} = -0.5mA	2.4			V
V _{OH2}	High-level output voltage 2	I _{OH} = -0.05mA	V _{cc} -0.5V			V
V _{OL}	Low-level output voltage	I _{OL} =2mA			0.4	V
I _I	Input current	V _I =0 ~ V _{cc}			±1	µA
I _O	Output current in off-state	S ₁ =V _{IH} or S ₂ =V _{IL} or OE=V _{IH} V _{I/O} =0 ~ V _{cc}			±1	µA
I _{cc1}	Active supply current (CMOS-level Input)	S ₁ 0.2V, S ₂ V _{cc} -0.2V, other inputs 0.2V or V _{cc} -0.2V,output-open	f= 10MHz f= 5MHz	20 10	25 13	mA
I _{cc2}	Active supply current (TTL-level Input)	S ₁ =V _{IL} ,S ₂ =V _{IH} , other inputs=V _{IH} or V _{IL} output-open	f= 10MHz f= 5MHz	22 12	27 15	mA
I _{cc3}	Stand-by current	1) S ₂ 0.2V or 2) S ₁ V _{cc} -0.2V, S ₂ V _{cc} -0.2V other inputs=0 ~ V _{cc}	-L -20 ~ +70°C -LL -20 ~ +40°C +25°C		60 10 1 0.6	µA
I _{cc4}	Stand-by current	S ₁ =V _{IH} or S ₂ =V _{IL} ,other inputs=0 ~ V _{cc}			0.33	mA

* -3.0V in case of AC (Pulse width 30ns)

CAPACITANCE

(T_a=0 ~ 70°C, V_{cc}= 2.7 ~ 3.6V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C _I	Input capacitance	V _I =GND, V _I =25mVrms, f=1MHz			7	pF
C _O	Output capacitance	V _O =GND, V _O =25mVrms, f=1MHz			9	pF

Note 1: Direction for current flowing into an IC is positive (no mark).

2: Typical value is for V_{cc} = 3V, T_a = 25°C

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AC ELECTRICAL CHARACTERISTICS

(Ta =0 ~ 70°C, Vcc= 2.7 ~ 3.6V, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

- Vcc 2.7 ~ 3.6V
- Input pulse level VIH=2.2V, VIL=0.4V
- Input rise and fall time 5ns
- Reference level VOH=VOL=1.5V
- Output loads Fig.1, CL=30pF
CL=5pF (for ten, tdis)

Transition is measured ±500mV from steady state voltage. (for ten, tdis)

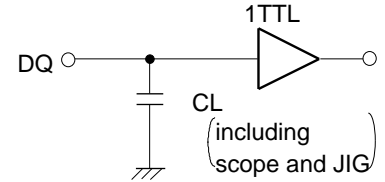


Fig.1 Output load

(2) READ CYCLE

Symbol	Parameter	Limits								Unit
		-70L,LL		-85L,LL		-10L,LL		-12L,LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCR	Read cycle time	70		85		100		120		ns
ta(A)	Address access time		70		85		100		120	ns
ta(S1)	Chip select 1 access time		70		85		100		120	ns
ta(S2)	Chip select 2 access time		70		85		100		120	ns
ta(OE)	Output enable access time		35		45		50		60	ns
tdis(S1)	Output disable time after S1 high		25		30		35		40	ns
tdis(S2)	Output disable time after S2 low		25		30		35		40	ns
tdis(OE)	Output disable time after OE high		25		30		35		40	ns
ten(S1)	Output enable time after S1 low	10		10		10		10		ns
ten(S2)	Output enable time after S2 high	10		10		10		10		ns
ten(OE)	Output enable time after OE low	5		5		5		5		ns
tv(A)	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

Symbol	Parameter	Limits								Unit
		-70L,LL		-85L,LL		-10L,LL		-12L,LL		
		Min	Max	Min	Max	Min	Max	Min	Max	
tCW	Write cycle time	70		85		100		120		ns
tw(W)	Write pulse width	55		60		75		85		ns
tsu(A)	Address setup time	0		0		0		0		ns
tsu(A-WH)	Address setup time with respect to W	65		70		85		100		ns
tsu(S1)	Chip select 1 setup time	65		70		85		100		ns
tsu(S2)	Chip select 2 setup time	65		70		85		100		ns
tsu(D)	Data setup time	30		35		40		45		ns
th(D)	Data hold time	0		0		0		0		ns
trec(W)	Write recovery time	0		0		0		0		ns
tdis(W)	Output disable time from W low		25		30		35		40	ns
tdis(OE)	Output disable time from OE high		25		30		35		40	ns
ten(W)	Output enable time from W high	5		5		5		5		ns
ten(OE)	Output enable time from OE low	5		5		5		5		ns

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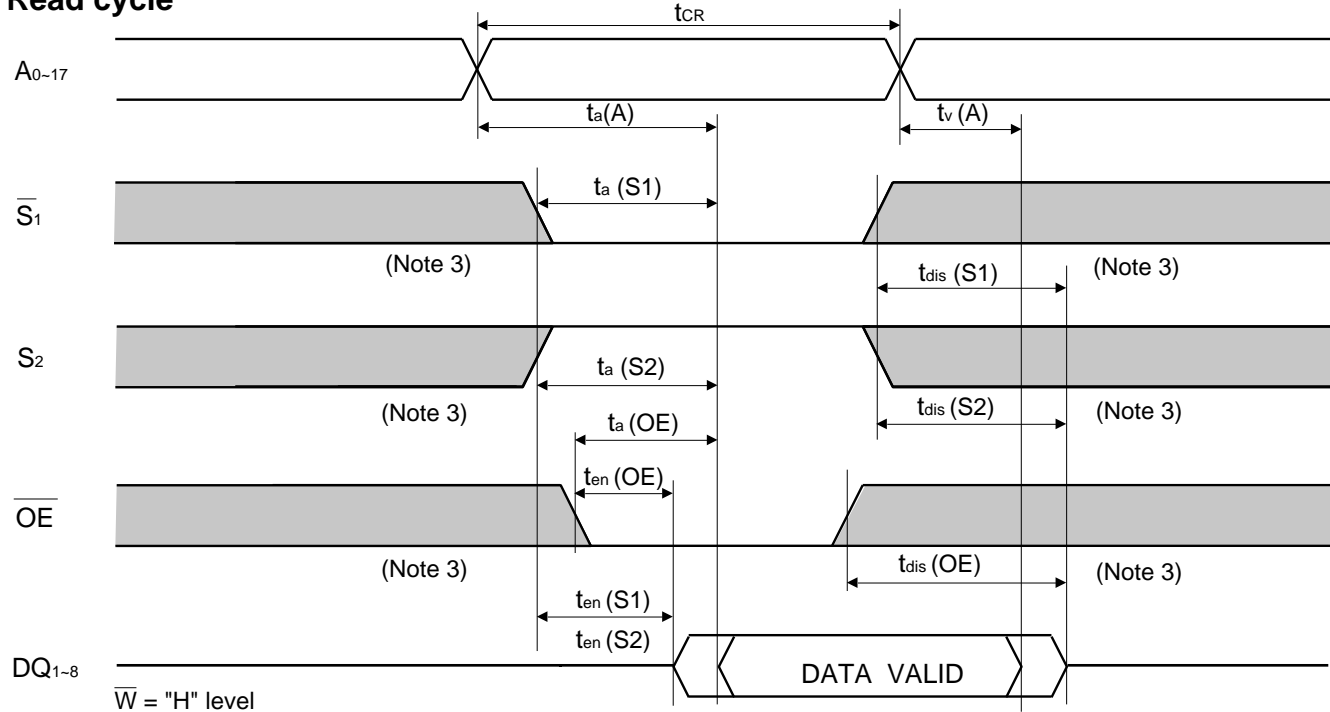
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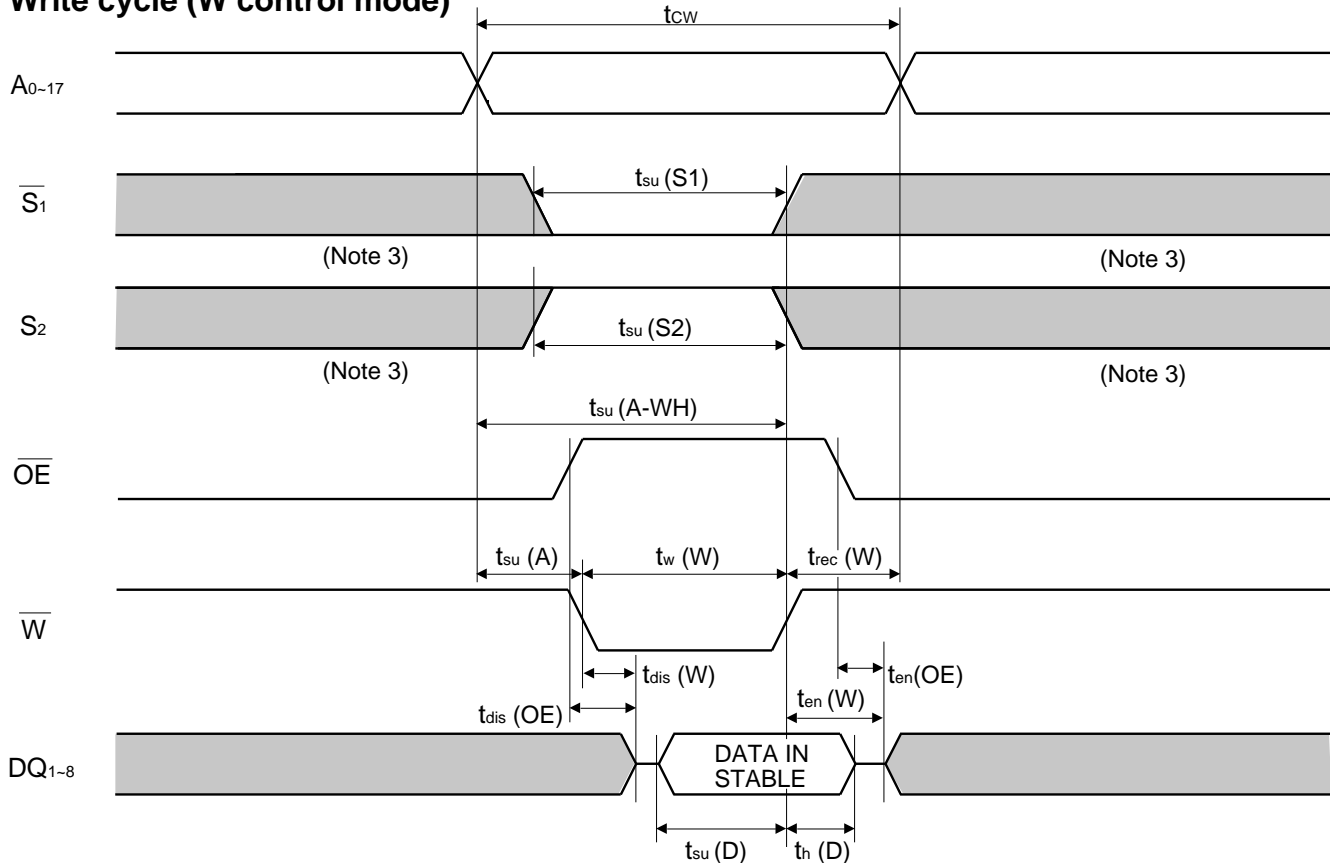
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(4) TIMING DIAGRAMS

Read cycle



Write cycle (\overline{W} control mode)



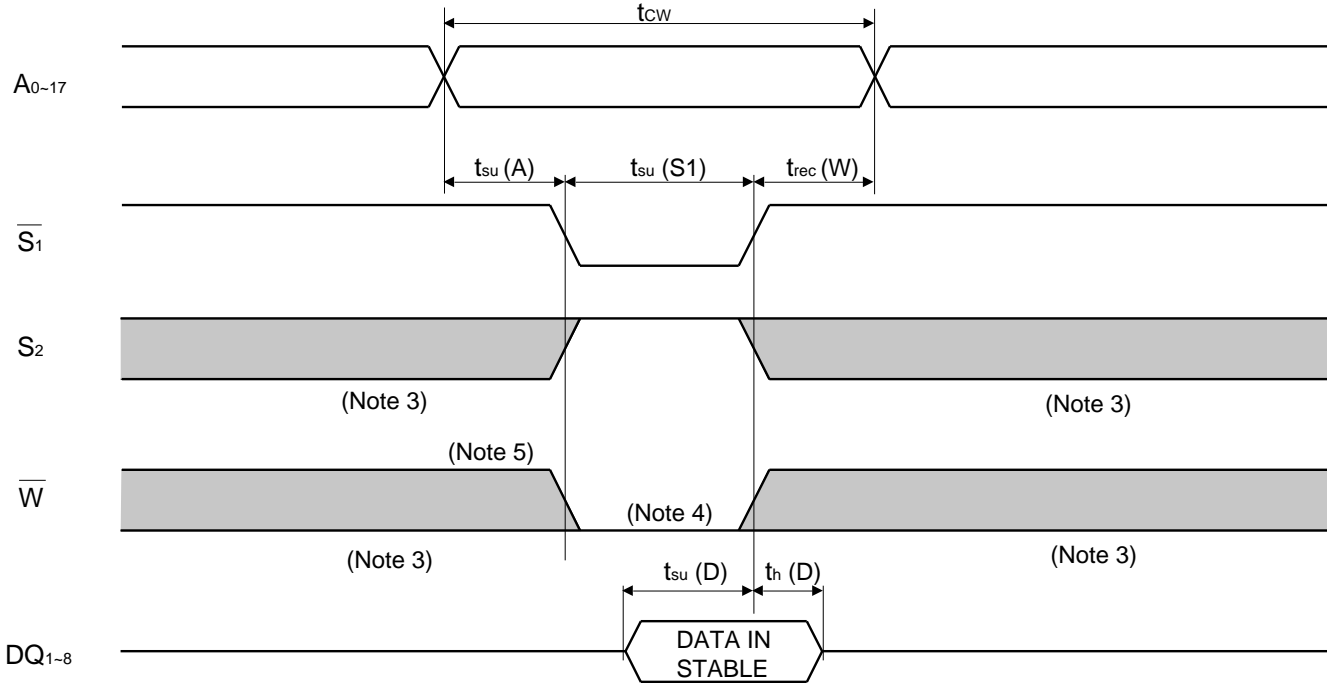
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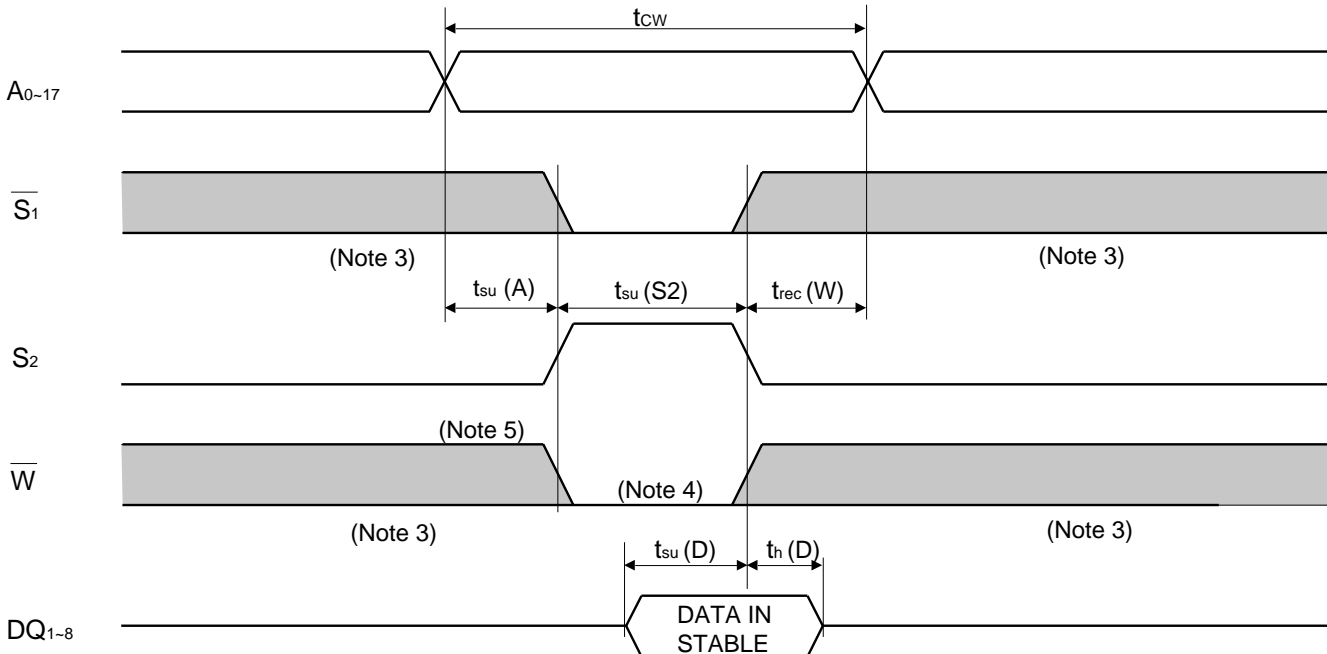
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Write cycle ($\overline{S1}$ control mode)



Write cycle ($S2$ control mode)



- Note 3: Hatching indicates the state is "don't care".
- 4: Writing is executed while $S2$ high overlaps $S1$ and \overline{W} low.
- 5: When the falling edge of \overline{W} is simultaneously or prior to the falling edge of $\overline{S1}$ or rising edge of $S2$, the outputs are maintained in the high impedance state.
- 6: Don't apply inverted phase signal externally when DQ pin is output mode.

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POWER DOWN CHARACTERISTICS

(1) ELECTRICAL CHARACTERISTICS

(Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V _{CC (PD)}	Power down supply voltage		2			V
V _{I (S1)}	Chip select input S ₁		2.0			V
V _{I (S2)}	Chip select input S ₂				0.2	V
I _{CC (PD)}	Power down supply current	V _{CC} = 3.0V S ₂ 0.2V or S ₁ V _{CC} - 0.2V, S ₂ V _{CC} - 0.2V	-L		50	μA
			-LL	0.3	8 <small>(Note 7)</small>	

Note7: I_{CC (PD)} = 0.5μA (Max.) in case of Ta = +25°C

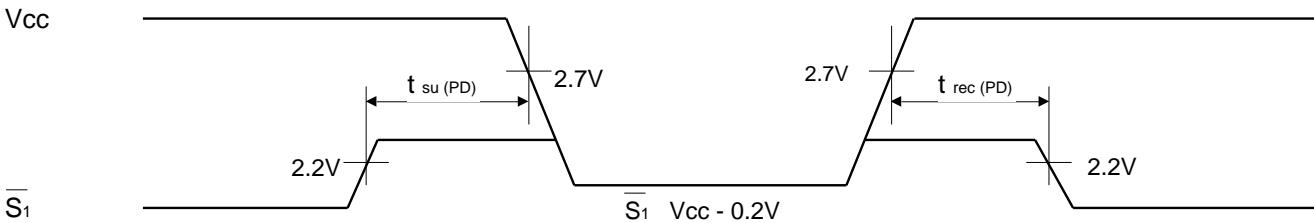
(2) TIMING REQUIREMENTS

(Ta = 0 ~ 70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
t _{su (PD)}	Power down set up time		0			ns
t _{rec (PD)}	Power down recovery time		5			ms

(3) POWER DOWN CHARACTERISTICS

S₁ control mode



S₂ control mode

